

computer systems. Therefore, it is the object of the appended claims to cover all such variations and modifications as come within the true spirit and scope of the invention.

What is claimed is:

## CLAIMS

1        1. In a computer system having one or more processors and one or more peripheral devices connected to an Input/Output (I/O) bus, an I/O bridge coupled to the I/O bus and configured to interface between the one or more processors and the one or more peripheral devices, the I/O bridge comprising:

5              a queue for buffering information received from the one or more processors; and  
6              a transaction engine operably coupled to the queue, the transaction engine config-  
7          ured to place information buffered at the queue onto the I/O bus for receipt by a targeted  
8          peripheral device,

9              wherein the transaction engine:

10              generates an attribute message that includes a tag field and a requester  
11          function number field,

12              loads the tag field with a selected value,

13              loads the requester function number field with a selected one of a plurality  
14          of values, and

15              places the attribute message including the selected tag and requester func-  
16          tion number values onto the I/O bus for receipt by the targeted I/O device.

1        2. The I/O bridge of claim 1 wherein the transaction engine logically concatenates  
2          the tag field and the requester function number field of the attribute message to create a  
3          super tag value for use in tracking transactions placed on the I/O bus.

1        3. The I/O bridge of claim 2 wherein the super tag ranges from binary  
2          “00000000” to binary “11111111”.

1        4. The I/O bridge of claim 1 wherein the queue has a plurality of entries for buff-  
2          ering the information and each queue entry is associated with a corresponding tag value  
3          and a corresponding requester function number value.

1       5. The I/O bridge of claim 4 wherein, in response to a Split Completion Message  
2 containing a tag value and a requester function number value, the transaction engine uses  
3 the received tag and requester function number values to identify a corresponding queue  
4 entry and clears the identified entry.

1       6. The I/O bridge of claim 5 wherein the I/O bus operates in substantial compli-  
2 ance with the Peripheral Component Interface Extended (PCI-X) specification standard.

1       7. The I/O bridge of claim 4 wherein the transaction engine is further configured  
2 to place information received from a peripheral device along with a Split Completion  
3 transaction that specifies a tag value and a requester function number value into the queue  
4 entry associated with the specified tag and request function number values.

1       8. The I/O bridge of claim 7 wherein the information buffered at the queue com-  
2 prises at least one of command, address and data, and the command may be read or write.

1       9. The I/O bridge of claim 1 wherein the queue includes a read buffer for buffer-  
2 ing data that was received from a peripheral device and a write buffer for buffering in-  
3 formation that is to be provided to a targeted peripheral device.

1       10. The I/O bridge of claim 1 wherein the I/O bus operates in substantial compli-  
2 ance with the Peripheral Component Interface Extended (PCI-X) specification standard.

1       11. A method for use in a computer system having one or more processors, one or  
2 more memory subsystems, and one or more peripheral devices connected to an In-  
3 put/Output (I/O) bus, the method comprising the steps of:

4           providing at least one queue having a plurality of entries for buffering information  
5 received from or to be sent to a targeted peripheral device;

6           associating each queue entry with a selected tag value and with one of a plurality  
7 of selected requester function number values;

8           buffering information received from a processor or a memory subsystem in a se-  
9       lected queue entry;  
10          generating an attribute message that includes a tag field and a requester function  
11       number field;  
12          loading the tag field of the attribute message with the tag value associated with  
13       the selected queue entry;  
14          loading the requester function number field of the attribute message with the re-  
15       quester function number value associated with the selected queue entry; and  
16          placing the attribute message including the tag and requester function number  
17       values onto the I/O bus for receipt by the targeted I/O device.

1           12. The method of claim 11 further comprising the steps of:  
2           receiving a Split Completion transaction from a targeted peripheral device speci-  
3       fying a tag value and a requester function number value and including data;  
4           utilizing the received tag and requester function number values as an index to  
5       identify a corresponding queue entry; and  
6           buffering the data received from the targeted peripheral device at the identified  
7       queue entry.

1           13. The method of claim 11 further comprising the step of logically concatenating  
2       the tag field and the requester function number field of the attribute message to create a  
3       super tag value for use in tracking transactions placed on the I/O bus, wherein the super  
4       tag ranges from binary “00000000” to binary “11111111”.

1           14. The method of claim 13 wherein the I/O bus operates in substantial compli-  
2       ance with the Peripheral Component Interface Extended (PCI-X) specification standard.

1           15. The method of claim 14 wherein the information buffered at the queue com-  
2       prises at least one of command, address and data, and the command may be read or write.